# Abstracts

## Analysis of High-Speed GaAs Source-Coupled FET Logic Circuits

*M. Idda, T. Takada and T. Sudo. "Analysis of High-Speed GaAs Source-Coupled FET Logic Circuits." 1984 Transactions on Microwave Theory and Techniques 32.1 (Jan. 1984 [T-MTT]): 5-10.*

A source-coupled FET logic (SCFL) circuit is proposed for gigabit rate digital signal processing. FET threshold voltage tolerance in the SCFL circuit and the SCFL circuit performance are presented. The speed of the SCFL gate depends on the operating region of the FET. For high-speed operation, FET's drain-to-source voltage higher than a pinchoff voltage has to be supplied. The SCFL gate, which is composed of 1.5-μm gate-length FET's, shows that the minimum propagation time is predicted to be 25 ps/gate. Minimum rise time and fall time are expected to be 54 ps and 51 ps, respectively. Maximum RZ data rate is expected to be 5.6 Gb/s. The SCFL circuit is applicable for high-speed dlgital sigmd processing.

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